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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,764	10/02/2003	Xiang-Dong Mi	01333	9128

7590 03/14/2007

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,764	MI, XIANG-DONG	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10-03-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10-02-2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

2. Status: Please all replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 10-02-2003 under new application, which have been placed of record in the file. Claims 1-12 are pending in this action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang, Xiao-Yang et al. (US 2005/0083284 A1).

Regarding Claim 1, Huang, Xiao-Yang teaches a method of driving an active matrix cholesteric liquid crystal display (page 3, paragraph 36, Lines 1-5)) that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active

switching elements (page 3, paragraph 36, Lines 1-5, page 6, paragraph 6, Lines 1-5, see figure 6), a pixel being capable of producing two or more gray levels (page 6, paragraph 68 on the right side Lines 1-6), comprising: a) providing a select voltage and a plurality of data voltages (page 6, paragraph 70, Lines 1-6); and b) during a pixel writing cycle, applying the select voltage and the data voltages to the select (page 6, paragraph 70, Lines 1-6, page 7, paragraph 82) and data lines of the display to produce only three pixel voltage levels 0, +U and -U, having respective duty cycles (please see figure 5a, page 5, paragraph 57,58) and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels (please see figure 5a, page 5, paragraph 57,58, page 5, paragraph 53, Lines 5-8, gray scale is represented by amplitude modulation, page 6, paragraphs 70,71 and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)), and wherein the average voltage applied to a pixel during the pixel writing cycle is zero (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 2, Huang, Xiao-Yang teaches the data voltage levels consist of a zero voltage and a non-zero voltage U (please see figure 5a, page 5, paragraph 57,58, whereon off state zero voltage and on state is non-zero voltage).

Regarding Claim 3, Huang, Xiao-Yang teaches the active matrix liquid crystal display further includes a common electrode connected to all of the pixels, and further comprising the step of applying the zero voltage to the common electrode (please see figure 5a, page 5, paragraph 57,58, teaches pixel is driven to zero voltage, two electrodes are inheritant to a pixel,

one connected to data side and second to maintain appropriate voltage across pixel a common electrode) and the voltage U to the data line to generate the pixel voltage U, and applying the voltage U to the common electrode and the voltage to the data line to generate the pixel voltage – U (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 4, Huang, Xiao-Yang teaches the data voltage levels consist of a zero voltage and two non-zero voltages +U and -U (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 5, Huang, Xiao-Yang teaches the active matrix liquid crystal display further includes a common electrode connected to all of the pixels (please see figure 5a, page 5, paragraph 57,58, teaches pixel is driven to zero voltage, two electrodes are inheritant to a pixel, one connected to data side and second to maintain appropriate voltage across pixel a common electrode), and further comprising the step of applying the zero voltage to the common electrode (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 6, Huang, Xiao-Yang teaches a pixel writing cycle (page 6, paragraph 70, Lines 1-6, page 7, paragraph 82) a) a selection portion wherein a non zero pixel voltage is applied to any pixels in the display whose state is to be changed (please see figure 5a, page 5, paragraph 57,58); and b) a duty cycle portion wherein the duty cycle of the non zero pixel

voltages are determined (please see figure 5a, page 5, paragraph 57,58, gray scale is represented by amplitude modulation, page 6, paragraphs 70,71 and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)).

Regarding Claim 7, Huang, Xiao-Yang teaches a method of driving an active matrix cholesteric liquid crystal display (page 3, paragraph 36, Lines 1-5)) that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements (page 3, paragraph 36, Lines 1-5, page 6, paragraph 6, Lines 1-5, see figure 6), a pixel being capable of producing two or more gray levels (page 6, paragraph 68 on the right side Lines 1-6), comprising: a) providing a select voltage and a plurality of data voltages (page 6, paragraph 70, Lines 1-6); and b) during a pixel writing cycle, applying the select voltage and the data voltages to the select (page 6, paragraph 70, Lines 1-6, page 7, paragraph 82) and data lines of the display to produce only three pixel voltage levels 0, +U and -U, having respective duty cycles (please see figure 5a, page 5, paragraph 57,58) and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels (please see figure 5a, page 5, paragraph 57,58, page 5, paragraph 53, Lines 5-8, gray scale is represented by amplitude modulation, page 6, paragraphs 70,71 and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)), and wherein the average voltage applied to a pixel during the pixel writing cycle is zero (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 8, Huang, Xiao-Yang teaches the data voltage levels consist of a zero voltage and a non-zero voltage U U (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 9, Huang, Xiao-Yang teaches the active matrix liquid crystal display further includes a common electrode connected to all of the pixels, and further comprising the step of applying the zero voltage to the common electrode (please see figure 5a, page 5, paragraph 57,58, teaches pixel is driven to zero voltage, two electrodes are inheritant to a pixel, one connected to data side and second to maintain appropriate voltage across pixel a common electrode) and the voltage U to the data line to generate the pixel voltage U, and applying the voltage U to the common electrode and the voltage to the data line to generate the pixel voltage – U (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 10, Huang, Xiao-Yang teaches the data voltage levels consist of a zero voltage and two non-zero voltages +U and -U (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 11, Huang, Xiao-Yang teaches the active matrix liquid crystal display further includes a common electrode connected to all of the pixels (please see figure 5a, page 5, paragraph 57,58, teaches pixel is driven to zero voltage, two electrodes are inheritant to a pixel, one connected to data side and second to maintain appropriate voltage across pixel a common

electrode), and further comprising the step of applying the zero voltage to the common electrode (please see figure 5a, page 5, paragraph 57,58, where average voltage per cycle e.g. ((+30) +(-30v)/2 =0), zero).

Regarding Claim 12, Huang, Xiao-Yang teaches a pixel writing cycle (page 6, paragraph 70, Lines 1-6, page 7, paragraph 82) a) a selection portion wherein a non zero pixel voltage is applied to any pixels in the display whose state is to be changed (please see figure 5a, page 5, paragraph 57,58); and b) a duty cycle portion wherein the duty cycle of the non zero pixel voltages are determined (please see figure 5a, page 5, paragraph 57,58, gray scale is represented by amplitude modulation, page 6, paragraphs 70,71 and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Doane; J. William et al. (US 6518944 B1) Combined cholesteric liquid crystal display and solar cell assembly device

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

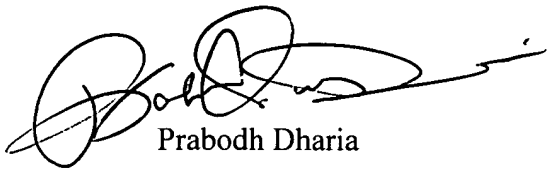
7. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Partial Signatory Authority

AU 2629

March 06, 2007